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Invention: METHOD FOR MANUFACTURING MOS TRANSISTOR AND SEMICONDUCTOR DEVICE EMPLOYING MOS TRANSISTOR MADE USING THE SAME

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SPECIFICATION

METHOD FOR MANUFACTURING MOS TRANSISTOR AND SEMICONDUCTOR DEVICE EMPLOYING MOS TRANSISTOR MADE USING THE SAME

BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to a method for manufacturing a MOS (metal-oxide-semiconductor) transistor of a semiconductor device. More particularly, the present invention relates to a method for manufacturing a MOS transistor that prevents contact spiking (i.e., excessive etching) of a field oxidation film adjacent to a device region during etching to form contact holes. The present invention relates also to a semiconductor device employing a MOS transistor manufactured using the method of the present invention.

(b) Description of the Related Art

There are two general classes of field effect transistors (FETs) and they include the MOSFET and the JFET (junction FET). The present invention is related to the MOSFET. The MOSFET typically includes on a semiconductor substrate the electrodes of a source, a drain, and a gate. Metal interconnect lines are connected to upper areas of the source, drain, and gate to allow application of electrical signals to the same, and the electrodes and the metal interconnect lines are electrically connected through contact formed at contact hole.

In order to minimize the resistance of each of the electrodes, silicide films are formed between the metal interconnect lines and each electrode of the source, drain, and gate. A silicon nitride film, which functions as an etching completion layer during etching to form contact holes, is deposited over an entire upper surface of the transistor that includes the silicide films.

FIGS. 1A to 1D are partial sectional views used to describe a conventional method for manufacturing a MOS transistor.

With reference to FIG. 1A, thermal oxidation of a silicon wafer 1, on which a device region is defined, is performed by a field oxidation film 2 using a LOCOS (local oxidation of silicon) or trench process such that a gate oxidation film 3 is grown on a surface of the device region of the silicon wafer 1. After depositing polysilicon, which will be used for gate electrodes 4, over an entire upper surface of the silicon wafer 1, the polysilicon and the gate oxidation layer 3 are patterned to a predetermined width.

Next, a p-type or n-type dopant is ion-injected at a low concentration on the device region of the silicon wafer 1 using a mask. As a result, LDDs (lightly doped drains) 5 are formed on the device region of the silicon wafer 1, as are side walls 6 to both sides of the gate oxidation film 3 and the gate electrode 4. Following this operation, a conducting dopant identical to that used for the LDDs 5 is ion-injected at a high concentration on the device region of the silicon wafer 1 using a mask to thereby form a source 7 and a drain 7.

Subsequently, titanium 8 is deposited to a thickness of approximately 400 Å over the entire surface of the silicon wafer 1 by a sputtering method, then RTP (rapid thermal processing) is performed for about 30 seconds and at a temperature of roughly 750℃ while injecting nitrogen at a flow rate of approximately 50 sccm. As a result, with reference to FIG. 1B, titanium silicide 8′ is formed by the reaction between titanium and silicon. The titanium on the side walls 6 and the field oxidation film 2 is not reacted and therefore remains as unreacted titanium 8.

The unreacted titanium 8 is a metal and so may interfere with device operation. The unreacted titanium 8 is therefore removed using a solvent. Also, in

order to reduce the resistance of the silicide 8' and increase the strength of the same, a heat process is performed in a nitrogen environment and at a temperature of approximately 910℃.

After the above processes, in order to form a liner film that is used as an etching completion layer during etching to form contact holes, a silicon nitride film 9, with reference to FIG. 1C, is formed to a thickness of roughly 300Å using plasma enhanced chemical vapor deposition (PECVD).

In the above process, the silicon nitride film 9 is less thickly deposited at depressed areas adjacent to the device region (one of which is circled using a dotted line in FIG. 1C) than in other areas. The depressed areas are formed as a result of structural problems occurring when forming the field oxidation film 2.

Next, an insulating layer, that is, a pre-metal dielectric (PMD) layer 10 is thickly formed by using atmospheric pressure chemical vapor deposition (APCVD) on the silicon nitride film 9, after which the PMD layer 10 is heat treated to improve the strength of the same. Chemical mechanical polishing (CMP) is then performed to flatten the PMD layer 10.

Subsequently, to prepare for the formation of contact holes, a photosensitive film pattern 11 is formed on the flattened PMD layer 10. With reference to FIG. 1D, exposed areas of the PMD layer 10 are then etched using the photosensitive film pattern 11 as a mask to thereby form contact holes 12.

Next, TiN 13 is then thinly deposited as a barrier metal film over the entire upper surface of the silicon wafer 1, after which tungsten 14 is used to fill the contact holes 12.

In the above conventional method for manufacturing a MOS transistor, the

silicon nitride film 9, which is used as an etching completion layer, is not formed to a uniform thickness. As a result, when etching the PMD layer 10, the areas of the silicon nitride film 9 formed over the depressed areas of the field oxidation film 2 adjacent to the device region are more quickly etched than other areas of the silicon nitride film 9. Therefore, a contact spiking phenomenon occurs, in which the silicon nitride film 9 is over-etched past where the field oxidation film 2 (under these areas of the silicon nitride film 9) starts. One such area is circled using a dotted line in FIG. 1D. The contact spiking phenomenon ultimately results in the interference of the flow of current in the source 7 and the drain 7 such that the semiconductor device operates improperly.

Such a contact spiking phenomenon may also occur as a result of mis-alignment of the photosensitive film pattern 11 when forming the same to form the contact holes 12.

SUMMARY OF THE INVENTION

It is an advantage of the present invention to provide a method for manufacturing a MOS (metal-oxide-semiconductor) transistor of a semiconductor device that prevents the occurrence of the contact spiking phenomenon in which a field oxidation film is excessively etched during etching of an insulating layer in order to form contact holes.

It is another advantage of the present invention to provide a semiconductor device employing a MOS transistor manufactured using the method of the present invention.

In the present invention, part of an unreacted metal thin film that is unused when forming silicide is left remaining over a field oxidation film such that excessive

etching of the same is prevented.

In one embodiment, the present invention includes a method for manufacturing a metal-oxide-semiconductor transistor. The method includes forming a metal thin film and an isolation oxidation film on a semiconductor substrate, and selectively etching the isolation oxidation film such that the isolation oxidation film is left remaining only over a field oxidation film; heat treating the semiconductor substrate to form silicide by the metal thin film in gate, source, and drain regions; removing portions of the metal thin film that is not formed into silicide, that is, removing unreacted metal thin film; removing the isolation oxidation film left remaining on the field oxidation film; and heat treating the semiconductor substrate in an oxygen environment to form the unreacted metal thin film remaining on the field oxidation film into a metal oxidation film.

Preferably, the isolation oxidation film is formed by performing deposition to a thickness of 300~500Å using plasma enhanced chemical vapor deposition, and the metal oxidation film is formed by performing rapid thermal processing in an oxygen environment, at a temperature of 700~800℃, and for 20~40 seconds.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principles of the invention.

FIGS. 1A to 1D are partial sectional views used to describe a conventional method for manufacturing a MOS transistor.

FIGS. 2A to 2E are partial sectional views used to describe a method for manufacturing a MOS transistor according to an embodiment of the present invention.

DETAILED DESCRIPTION

Embodiments of the present invention will now be described in detail with reference to the accompanying drawings.

FIGS. 2A to 2E are partial sectional views used to describe a method for manufacturing a MOS (metal-oxide-semiconductor) transistor according to an embodiment of the present invention.

With reference first to FIG. 2A, a field oxidation film 22 is formed on a predetermined region of a silicon wafer 21 using a LOCOS (local oxidation of silicon) or a trench process. The predetermined region of the silicon wafer 21 where the field oxidation film 22 is formed is referred to as a device separation region, while all other areas are referred to as a device region. A gate oxidation film 23 is grown on a surface of the silicon wafer 21 in the device region by performing thermal oxidation of the silicon wafer 21.

Next, polysilicon is deposited over an entire surface of the silicon wafer 21 on a side of the same on which the gate oxidation film 23 is grown, thereby forming a gate electrode 24. Using the gate electrode 24 as a mask, a p-type or n-type dopant is ion-injected in the device region of the silicon wafer 21 such that LDDs (lightly doped drains) 25 are formed on the silicon wafer 21, and side walls 26 are formed to both sides of the gate oxidation film 23 and the gate electrode 24. Following this procedure, a conducting dopant identical to that used for the LDDs 25 is ion-injected at a high concentration on the device region of the silicon wafer 21 using the side walls 26 and the gate electrode 24 as a mask to thereby form a source 27 and a drain 27.

Subsequently, using a sputtering method, titanium 28 is deposited to a thickness of approximately 300~500Å over the entire surface of the silicon wafer 1 on

which the source 27 and drain 27 are formed, then an isolation oxidation film 29 is formed over the titanium 28 using PECVD (plasma enhanced chemical vapor deposition) to a thickness of roughly 800~1200Å. Preferably, the titanium is deposited to a thickness of 400Å and the isolation oxidation film 29 is deposited to a thickness of 1000Å. Cobalt may be used in place of the titanium 28.

Following the above processes, a photosensitive film is deposited on the isolation oxidation film 29, then this film is exposed and developed to thereby form a counter active pattern 30 that exposes only the device region. The counter active pattern 30 is then used as a mask to perform wet etching of the isolation oxidation film 29 and remove the same. Therefore, the isolation oxidation film 29 is left remaining only over the field oxidation film 22 as shown in FIG. 2B.

Next, RTP (rapid thermal processing) is performed for about 20~40 seconds at a temperature of roughly 700~800℃ while injecting nitrogen at a flow rate of approximately 50 sccm. As a result, titanium silicide 28′ is formed by the reaction between the titanium 28 and silicon. The preferable temperature and time of performing RTP for the formation of the titanium silicide 28′ are 750℃ and 30 seconds, respectively. The titanium 28 covering the side walls 26 and the field oxidation film 22 is unable to be reacted with the silicon and so remains as unreacted titanium 28.

Following the above, the unreacted titanium 28 is removed. In this regard, since the unreacted titanium 28 that covers the field oxidation film 22 is itself covered by the isolation oxidation film 29, only the unreacted titanium 28 that covers the side walls 26 is extracted in this removal process as shown in FIG. 2C. The isolation oxidation layer 29 left remaining over the field oxidation film 22 is then removed using a solvent.

Subsequently, RTP is performed for about 20～40 seconds at a temperature of roughly 700～800℃ while injecting oxygen at a flow rate of approximately 50 sccm. Hence, the unreacted titanium 28 over the field oxidation film 22 is oxidized and formed into a titanium oxidation film 31 as shown in FIG. 2D. The preferable temperature and time of performing RTP for the formation of the titanium oxidation film 31 are 750℃ and 30 seconds, respectively. In this process, the titanium silicide 28' in the device region undergoes almost no reaction with the oxygen. Next, in order to reduce the resistance of the titanium silicide 28' and increase the strength of the same, a heat process is performed in a nitrogen environment, at a temperature of approximately 850～950℃, and for 5～15 seconds, preferably at a temperature of 910℃ and for 10 seconds.

Following the above, in order to form a film for use as an etching completion layer during etching to form contact, a silicon nitride film 32 is formed to a thickness of roughly 200～400Å using PECVD. The silicon nitride film 32 is preferably formed to a thickness of 300Å.

Next, an insulating layer, that is, a PMD (pre-metal dielectric) layer 33 is thickly formed on the silicon nitride film 32 using APCVD (atmospheric pressure chemical vapor deposition), after which the PMD layer 33 is heat treated at a temperature of 600～800℃ for 30～50 seconds such that the strength of the PMD layer 33 is increased. CMP (chemical mechanical polishing) is then performed to flatten the PMD layer 33. Heat treating of the PMD layer 33 is preferably performed at a temperature of 700℃ and for 40 seconds.

Subsequently, to prepare for the formation of contact holes, a photosensitive film pattern 34 is formed on the flattened PMD layer 33. Next, with reference to FIG. 2e,

exposed areas of the PMD layer 33 are etched using the photosensitive film pattern 34 as a mask to thereby form contact holes 35. Since the titanium oxide film 31 is formed on the field oxide film 22, excessive etching of the field oxide film 22 where the field oxide film 22 is depressed adjacent to the device region is avoided.

TiN 36 is then thinly deposited as a barrier metal film over the entire surface of the silicon wafer 21 on which the above elements are formed, after which tungsten 37 is used to cover all elements and fill the contact holes 35.

Further, a metal thin film (not shown) is deposited and patterned on the PMD layer 33 such that a metal wiring layer (also not shown) that connects to tungsten plugs filling the contact holes 35 is formed. This completes the semiconductor device.

In the method for manufacturing a MOS transistor according to the embodiment of the present invention described above, the isolation oxidation film is used so that unreacted titanium is left remaining on the field oxidation film, and the remaining unreacted titanium is oxidized to form the titanium oxidation film. As a result, the present invention prevents contact spiking in which there occurs excessive etching (into even the field oxidation layer adjacent to the device region) caused by the formation of depressions in the field oxidation film itself during the process of etching to form the contact holes or mis-alignment of the photosensitive film pattern. Therefore, current leakage and mis-operation of the device caused by contact spiking are prevented.

Although embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the spirit and scope of the present

invention, as defined in the appended claims.